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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/825,910 | 04/16/2004 | Byung Tai Do | 27-017 | 8877 |

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| EXAMINER | |
|---|---|
| HO, TU TU V | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2818 | |

DATE MAILED: 02/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) |
|---|---|---|
| | 10/825,910 | DO ET AL. |
| | Examiner | Art Unit |
| | Tu-Tu Ho | 2818 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *19 September 2005 and 01 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 August 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. As mentioned in the Requirement for Restriction/Election mailed 09/30/2005, the finality of the rejection of the office action mailed 06/17/2005 has been withdrawn and prosecution on the merits of this application has been reopened. Additionally, in response to Applicant's arguments to the 09/30/2005 Restriction Requirement in the Appeal Brief field 12/01/2005, said Restriction Requirement is hereby withdrawn because said arguments have been found persuasive.

### *Claim Rejections - 35 USC § 102*

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

**2. Claims 16-18, 6-8, 11-13, 15, 1-3, and 5** are rejected under 35 U.S.C. 102(e) as being anticipated by Chung et al. U.S. Patent Application Publication 20040183180 (hereinafter the '180 reference).

The '180 reference discloses in the figures, particularly Figs. 3 and 5, and respective portions of the specification a semiconductor package as claimed.

Referring to **claim 16**, the '180 reference discloses a thermally enhanced semiconductor package with a stack of dies comprising:

a heat sink ("supporter" 35, paragraph [0021], which can be a heat spreader, paragraph [0023], Fig. 5) between dies ("chips" 34 and 32) in the stack;

the heat sink having a body portion (352), an undercut portion (generally indicated at a portion of supporting portion, or leg 354) around a periphery thereof, and a plurality of legs ("slant columns", paragraph [0021]: "the supporting portion 354 may be a ring or is composed of slant columns connecting to the carrying portion") integrally formed with the undercut portion.

Referring to **claim 17**, the reference further discloses that the undercut of the heat sink extends laterally over the die to which the heat sink is attached (as clearly depicted in Fig. 5).

Referring to **claim 18**, the reference further discloses that the heat sink is electrically grounded (paragraph [0024]).

Referring to **claim 6** and using the same reference characters, interpretations, and citations as detailed above for claim 16 where applicable, the reference discloses a thermally enhancing a semiconductor package with a stack of dies and an inherent method of thermally enhancing a semiconductor package with a stack of dies, the method comprising providing a heat sink between dies in the stack; the heat sink having a body portion, an undercut portion around a periphery thereof, and a plurality of legs integrally formed with the undercut portion.

Referring to **claim 7**, the reference further discloses providing a heat sink attaches a heat sink that extends laterally over the lower die to which the heat sink is attached (as clearly depicted in Fig. 5).

Referring to **claim 8**, the reference further discloses that providing a heat sink attaches a heat sink that is electrically grounded (paragraph [0024]).

Referring to **claim 11** and using the same reference characters, interpretations, and citations as detailed above for claim 16 where applicable, the reference discloses a semiconductor package with stacked dies comprising:

a substrate (36, Fig. 3, no number in Fig. 5); a

first die attached to the substrate;

the first die being electrically connected to the substrate;

a heat sink attached to the first die (Fig. 5);

the heat sink having a body portion, an undercut portion around a periphery thereof, and a plurality of legs integrally formed with the undercut portion;

the plurality of legs attached to the substrate;

a second die attached to the heat sink and electrically connected to the substrate; and

an encapsulant (no number in Fig. 5, 39 in Fig. 3, paragraph [0021]) over the first die, the heat sink, and the second die.

Referring to **claim 12**, the reference further discloses a number of bonding wires (no number in Fig. 5, 37 in Fig. 3, paragraph [0021]) electrically connecting the first die to the substrate; and

wherein:

the undercut of the heat sink extends laterally over the number of bonding wires (as best seen in Fig. 5).

Referring to **claim 13**, the reference further discloses that the heat sink is electrically grounded (paragraph [0024]).

Referring to **claim 15**, the reference further discloses that the undercut of the heat sink extends laterally beyond the edges of the second die (32) (as best seen in Fig. 5).

Referring to **claim 1** and using the same reference characters, interpretations, and citations as detailed above for claims 16 and 11 where applicable, the reference discloses a

semiconductor package with stacked dies and an inherent method of assembling a semiconductor package with stacked dies, the method comprising:

providing a substrate;

attaching a first die to the substrate;

electrically connecting the first die to the substrate;

attaching a heat sink to the first die;

the heat sink comprising a body portion, an undercut portion around a periphery thereof, and a plurality of legs integrally formed with the undercut portion;

attaching the plurality of legs to the substrate;

attaching a second die to the heat sink;

electrically connecting the second die to the substrate; and

encapsulating the fist die, the heat sink, and the second die.

Referring to **claim 2**, the reference further discloses that electrically connecting the first die to the substrate uses a number of bonding wires (no number in Fig. 5, 37 in Fig. 3, paragraph [0021]); and

attaching a heat sink attaches a heat sink that extends laterally over the number of bonding wires.

Referring to **claim 3**, the reference further discloses that attaching a heat sink attaches a heat sink that is electrically grounded (paragraph [0024]).

Referring to **claim 5**, the reference further discloses that attaching a heat sink attaches a heat sink that extends laterally beyond the edges of the second die (32) (as best seen in Fig. 5).

***Claim Rejections - 35 USC § 103***

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. **Claims 20 and 10** are rejected under 35 U.S.C. §103(a) as being unpatentable over Chung et al. U.S. Patent Application Publication 20040183180 (the '180 reference).

The '180 reference discloses a semiconductor package and an inherent method of assembling the semiconductor package as claimed and as detailed above for claims 16 and 6, including a heat sink positioned between the pair of dies in the stack of dies. However the reference does not disclose that a heat sink is positioned between each adjoining pair of dies in the stack of dies. In other words, the reference does not appear to teach stacking more than two dies wherein a heat sink is positioned between each adjoining pair of dies in the stack of dies. Nevertheless, as detailed, the reference teaches a semiconductor stack wherein a heat sink is positioned between the pair of dies in the stack of dies, and since it has been found that the addition of an element (a third or more die, another or more heat sink, as in the instant case) to a structure of two dies with a heat sink positioned between the pair of dies, which combination does not result in new or surprising function, involves only routine skill in the art and is not patentable.

4. **Claims 19, 9, 14, and 4** are rejected under 35 U.S.C. §103(a) as being unpatentable over Chung et al. U.S. Patent Application Publication 20040183180 (the '180 reference) in view of Shin et al. U.S. Patent 5,854,511 (the '511 reference, cited in a previous office action).

The '180 reference discloses a semiconductor package with stacked dies and a method of assembling and using thereof as claimed and as detailed above for claims 16, 18, 11, 13, 6, 8, 1, and 3, including the stack of dies (34,32) comprising the heat sink (35) having said undercut around its periphery between said dies in said stack of dies, wherein the heat sink is electrically grounded to the substrate (36) and the second die (32) is connected to the heat sink. However, the '180 reference does not disclose that the heat sink has an electrically conductive coating connected to a ground plane on the substrate, for the purpose of said electrically grounding of said heat sink, and consequently does not disclose that the second die is connected to the claimed electrically conductive coating.

Shin in the '511 reference, in disclosing a semiconductor package including a multilayered heat sink, teaches in the Abstract, Figs. 1 and 2, and column 1, lines 10-22, that an electrically conductive coating formed of silver or nickel and palladium as part of the heat sink results in an improvement in performance of the finally produced semiconductor package.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the heat sink of the '180 reference such that the heat sink has an electrically conductive coating. One would have been motivated to make such a modification in view of the Shin teachings that an electrically conductive coating formed of silver or nickel and palladium as part of the heat sink results in an improvement in performance of the finally produced semiconductor package. Thus the final modified package would have a heat sink having an electrically conductive coating connected to a ground plane on the substrate and that the second die would be connected to the electrically conductive coating as the second die is

connected to the heat sink which has the electrically conductive coating, in order to achieve an improvement in performance of the finally produced semiconductor package.

***Conclusion***

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
January 25, 2006